Claim Amendments

Claim 1 (currently amended): A switch for switching packets from a plurality of sources comprising:

a memory in which portions of packets are stored; and

a transferring mechanism which transfers predetermined portions of a packet to the memory as the predetermined portions are received, the transferring mechanism **[[16]]** transfers predetermined portions of the packet as fixed length segments as the fixed length segments are received followed by a single final segment of any length less than or equal to the length of the fixed length segments wherein the packet is transferred to the memory **[[14]]** to smooth out bursts caused by lengthy packets.

Claim 2 (canceled)

Claim 3 (previously presented): A switch as described in Claim 1 wherein the transferring mechanism transfers fixed length segments of different packets interleaved among each other as they are received to the memory.

Claim 4 (original): A switch as described in Claim 3 wherein the transferring mechanism includes an aggregator which receives portions of packets from the plurality of sources.

Claim 5 (original): A switch as described in Claim 4 wherein the memory includes a memory controller.

Claim 6 (original): A switch as described in Claim 5 wherein the aggregator uses TDM to multiplex segments of packets from different sources to the memory controller.

Claim 7 (original): A switch as described in Claim 6 wherein the aggregator places an identifier with each segment identifying from which source the segments came from.

Claim 8 (original): A switch as described in Claim 7 wherein the memory controller includes per source queues, and stores each segment in a corresponding per source queue based on the identifier of the segment.

Claim 9 (original): A switch as described in Claim 8 wherein the memory controller includes per destination queues, and once all segments for a packet are received at a

per source queue, all the segments of the packet are changed to a corresponding per destination queue.

Claim 10 (original): A switch as described in Claim 9 wherein the memory controller has acceptance criteria for accepting segments, and if the segment is not accepted, then all previously received segments associated with the segment not accepted are purged from the per source queue and any segments associated with the segment not accepted that are received after the segment that was not accepted was received, are ignored.

Claim 11 (original): A switch as described in Claim 10 including a fabric in which the aggregator and the memory controller are disposed, and including a separator disposed in the fabric connected to the aggregator.

Claim 12 (original): A switch as described in Claim 11 including a port card having a striper which sends portions of packets to the aggregator, and an unstriper which receives portions of packets from the separator.

Claim 13 (original): A switch as described in Claim 12 wherein the memory controller includes a shared memory, and the destination queues and the source queues are part of the shared memory.

Claim 14 (currently amended): A method for switching packets comprising the steps of:

receiving portions of a packet at a transferring mechanism of a switch; and

transferring predetermined portions of the packet to a memory as fixed length segments as the fixed length segments are received at the transferring mechanism **[[16]]** followed by a single final segment of any length less than or equal to the length of the fixed length segments wherein the packet is transferred to the memory **[[14]]** to smooth out bursts caused by lengthy packets.

Claim 15 (canceled)

Claim 16 (previously presented): A method as described in Claim 14 wherein the transferring step includes the step of transferring fixed length segments of different packets as they are received interleaved among each other to the memory.

Claim 17 (original): A method as described in Claim 16 wherein the receiving step includes the step of receiving portions of packets from different sources at an aggregator of the transferring mechanism disposed in a fabric of the switch.

Claim 18 (original): A method as described in Claim 17 wherein the transferring step includes the step of multiplexing with the aggregator segments of packets from different sources to the memory controller.

Claim 19 (original): A method as described in Claim 18 wherein before the transferring step, there is the step of placing by the aggregator an identifier with each segment identifying from which source the segment came from.

Claim 20 (original): A method as described in Claim 19 wherein after the transferring step, there is the step of storing each segment in a corresponding per source queue of the memory controller based on the identifier of the segment.

Claim 21 (original): A method as described in Claim 20 including after the storing step, there is the step of changing all segments of the packet in the source queue to a corresponding per destination queue of the memory controller once all the segments of the packet are received at the per source queue.

Claim 22 (original): A method as described in Claim 21 wherein the receiving step includes the steps of purging all previously received segments associated with an unaccepted segment that does not meet acceptance criteria for accepting a segment of the

memory controller, and ignoring all segments associated with the unaccepted segment received at the memory controller after the unaccepted segment is received at the memory controller.

Claim 23 (original): A method as described in Claim 22 wherein the receiving step includes the step of receiving portions of packets from different sources at the aggregator of the transferring mechanism disposed in the fabric of the switch from a striper of a port card of the switch.

Claim 24 (original): A method as described in Claim 23 including after the moving step, there is the step of sending portions of packets from the memory controller with a separator of the fabric to an unstriper of the port card.